Electrical Analysis and Design of Differential Pairs Used in High-Speed Flip-Chip BGA Packages

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Abstract — In the paper, electrical analysis and design of the differential pairs used in high-speed flip-chip ball grid array (FC-BGA) packages are presented in the frequency range up to 10GHz. The emphases are on the critical factors that determine the overall electrical performance of the differential pairs and the related packages including impedance control and the impact of discontinuities such as via and solder ball. Manufacturing tolerance is also considered in terms of characteristic impedance. The purposes of this paper are to give an insight into electrical aspects of practical differential pairs in the FC-BGA packages to speed up high-speed packaging design.

I. INTRODUCTION

Driven by the needs in communication and consumer electronics market, the trends of IC chips are toward miniaturization, low power consumption, high integration, and high data rate, which place increasingly high demands on interconnection performance [1, 2]. High-speed devices like the advanced memory buffer (AMB) in a fully buffered dual in-line memory module (FB-DIMM) operate at such high data rate that the related packages are responsible for the majority of signal degradation, and they need be designed in a broad frequency range up to several gigahertz [3, 4]. Hence, interconnection design for such a high-frequency and broadband packaging solution becomes a challenge, where previously negligible effects such as ringing, delay, attenuation, distortion, reflections, and crosstalk become critical in system performance [5]. On the other hand, it is important for industries to seek for low-cost packaging solutions with standard manufacturing processes. Among the most promising technologies, the flip-chip ball-grid array (FC-BGA) package combines high performance, relative low cost, high reliability, and relative simplicity [6]. This paper focuses on flip-chip BGA package.

The noise caused by external interference and crosstalk between traces increases with frequency, which degrades the quality of the signals propagating on the traces. Usually, high-speed signaling uses differential pairs in terms of coupled microstrip or stripline as the noise due to crosstalk and external interference is mostly presented as common mode and a differential receiver has the capability to suppress common noise. On the other hand, high-density and high-speed package has the size comparable to the wavelength of the highest interesting frequency. The differential pairs in those packages are electrically long so that they need be considered as the coupled transmission lines, usually used in microwave area [7, 8], which is important to control their characteristic impedance. The discontinuities like via and solder ball in high-speed differential pair have a critical impact on electrical performance, which are usually treated as a two-port network. Those discontinuities must be carefully analyzed and designed in order to meet the given electrical requirements. This paper makes the efforts on differential pair and the abovementioned concerns in high-speed FC-BGA package design with analytical analysis and numerical simulations.

II. 2D DIFFERENTIAL PAIR DESIGN

According to the stack-up of a high-speed package, the embedded coupled microstrip or stripline can be applied to implement differential pairs, usually whose electrical requirements are specified in terms of return loss. On the other hand, the frequency range concerned in a high-speed package is completely determined by rise/fall time of digital signal. Once the interesting frequency range and the length of an uniform differential pair in a package are known, the return loss of this uniform pair is related to its impedance

\[ RL = 20 \log_{10} \left( \frac{Z^2 - Z_0^2}{2Z_0 + Z} \right) \]

where, \( Z \) is the impedance of a differential pair and \( Z_0 \) is the targeted impedance that usually is 100ohms for most differential pairs. Those impedances are actually the characteristic impedance of transmission lines determined by its cross-section and the material used. \( \gamma \) and \( l \) is the complex propagation constant and the length of a uniform
differential pair. Hence the impedance need be first controlled to reach the required electrical performance in initial packaging design. Fig. 1 shows the design of a centered stripline differential pair with BT material, where the trace has the thickness \( t = 20 \text{um} \) and the typical widths \( w = 30 \text{um}, 50 \text{um}, \) and \( 70 \text{um} \). In Fig. 1, the trace spacing \( s \) is related to the BT dielectric height \( H \) in order to implement 100ohm differential impedance. It is found that at a given trace width, the 100ohm differential pair cannot be implemented if BT dielectric height is smaller than a specified value. This specific height responds to one that implements 50ohm single-ended when only a single stripline is presented. It is also found that the impedance is more sensitive to small trace spacing than large one with the fixed trace width because small trace spacing means strong coupling. Trace thickness has the impact on differential pair’s impedance through capacitance to ground plane and to the other trace. Fig. 2 shows the design with different trace thickness and width. The capacitive coupling increases with trace thickness, which decreases differential pair’s impedance. Hence, one must increase trace spacing or dielectric height, or reduce trace width to compensate this increased capacitive coupling. Impedance control of microstrip differential pairs is similar with that of stripline one, which is not presented here.

Package manufacturing has some tolerance that has an impact on package’s electrical performance. Fig. 3 shows impedance error due to relative manufacturing tolerance in terms of BT dielectric permittivity (DK) and height, trace width, trace thickness, and trace spacing for a design selected from Fig. 1 \( (t=30\text{um}, w=30\text{um}, s=87.112\text{um}, \) and \( H=90\text{um} \)). It is found that the impedance changes linearly with all relative tolerances and the DK tolerance has the largest impact.

Although return loss is related to the impedance with Eq. (1), it depends on the length of a uniform differential pair, too. As \( Z \) is very close to \( Z_0 \) in tolerance studies,

\[
RL \equiv 20 \log \left( \frac{|Z_1 - Z_0|}{|Z_1 + Z_0|} \right)
\]

In high-speed and high I/O packages, the longest trace normally has the length larger than a quarter of the shortest interesting wavelength, which indicates that the worst return loss in a typical package can be reached within the interesting frequency range. Eq. (3) is independent of trace length. In order to consider the effects of material loss and the operating frequency on return loss in tolerance studies of a centered stripline differential pair, 2D numerical simulations are implemented for one design used before at different frequencies with \( \pm 10\% \) relative tolerance of BT dielectric DK and height, trace width, trace thickness, and trace spacing. Complex characteristic impedance of this lossy transmission line is extracted. Using Eq. (3), return loss is shown in Fig. 4, where it is found that all the tolerance result in return loss below –25dB. However, return loss changes with frequency.

Insertion loss of a lossy differential transmission line implies the attenuation of signal’s power transferred between I/O pins in a high-speed package. For a uniform line, insertion loss can be calculated if both the impedance and complex propagation constant are known with the following formulation

\[
IL = \frac{2Z_0 Z_{IL}}{Z_0^2 + 4Z_{IL}^2} \text{erf} \left( \frac{2Z_{IL} \gamma l}{Z_0 Z_{IL}} \right)
\]

As mentioned before, \( Z \) is very close to \( Z_0 \) in a designed high-speed package, hence
\[ IL \equiv -8.68589 \alpha l \]  

where \( \alpha \) is the attenuation constant of a uniform transmission line. With 2D numerical simulation at different frequencies, the theoretically maximum permissible length of the lossy differential transmission line used before under the -0.5dB and -1dB insertion loss requirement is shown in Fig. 5. It might be pointed out that the other factors like discontinuities are not taken into account in this insertion loss. This length can be regarded as theoretical upper limitation in packaging design, and exceeding this length indicates that no package can meet the given requirement.

### III. VIA AND SOLDER BALL CONSIDERATION

The introduction of any discontinuities in high-speed differential pairs results in the increase of return loss and insertion loss. In the flip-chip BGA package, the largest discontinuities come from solder balls, vias connecting the traces in different layers, and the related pads and anti-pads. In the substrate-based package, two types of vias and the related pads are usually used. One lies in the prepreg layers with the thickness up to several tens micrometers. This via is usually fabricated using laser with the diameter up to several ten micrometers. The other lies in the core layer. As its thickness is up to several hundred micrometers, the via in this layer is usually fabricated mechanically whose size is larger than the first via. Those vias with different sizes in different layers is connected in a staggered way or a stack-up way, shown in Fig. 6. The size of the vias, the related pads and anti-pads as well as the connecting way affect electrical performance. Below, consider a 6-layer BGA package with the 800um-thicknesses core layer. The prepreg layers are all 45um thick. Two via connections with the staggered and stackup ways shown in Fig. 6 to connect stripline differential transmission line in the second layer to the solder balls are considered. They have the same diameters of vias, pads, and antipads. Using Ansoft HFSS, the simulated return loss with the frequencies up to 10GHz is shown in Fig. 7. It is found the stackup via interconnection has the better electrical performance in the whole frequency range although the improvement is limited. Hence, it is preferable in high-speed packaging design in terms of electrical performance. The reason that its overall performance is not yet good is due to large size change in the via, the related pad and anti-pad, and the solder ball. Usually, it is desirable to use small via and pads, and large anti-pads in a core layer to reduce capacitive coupling to the power/ground plane. However, those sizes cannot be changed arbitrarily due to manufacturability limitation. One example is solder ball whose size is usually specified by standardization organization like JEDEC. Under the manufacturing constraints, designing high-performance interconnect becomes a great challenge, especially when conventional low-cost manufacturing process is adopted. To design a differential via interconnection, one firstly decreases the diameter of the vias and its pads within the acceptable range of manufacturability. Then one further increases the diameters of the antipads in the 3rd to 6th layers. Fig. 8 shows the return loss of the stackup via connections in this 6-layer BGA package as one decreases the diameters of the vias and its pads within the acceptable range of manufacturability.
of via/pad and then further increases the diameter of antipad. It is found that the performance is improved.

In order to evaluate the impact of the via and the imperfectly differential transmission lines on the overall electrical performance of differential pair in an actual FC-BGA package, a centered stripline differential pair is simulated, shown in Fig. 9. It is designed to have 100ohm differential impedance using the method mentioned in section II. However, it is not straight due to limited package area in practical layout. Furthermore, the ground planes above and below the striplines are not integral, and small part of the striplines is uncovered with the ground plane in order to route other traces. Those situations are all taken into account in the model, and the neighboring traces are also kept into the model to include their effects. Return loss and insertion loss of this differential pair are shown in Fig. 10 and 11 respectively. By the way, in the paper, only differential-mode results are presented, and common mode and mode transformation is not considered. Two sections of this differential pair are studied separately to consider their

impact on overall electrical performance, among which one section includes via and solder ball (discontinuity part) while the other section is the centered stripline transmission line. It is found that the first part takes the main contribution to return loss. Hence, to push high-frequency electrical performance, it is necessary to first improve electrical performance of via and solder ball. This part has the loading effect on the latter (transmission line), which cause the moving of resonant points toward low frequency. It is found the return loss of the whole pair is less than –15dB up to 6GHz and –13dB up to 10GHz.

Fig. 9. The differential pair in a practical BGA package.

Fig. 10. The comparison of insertion loss of whole differential pair, via/solder ball section, and stripline section respectively.

Fig. 11. The comparisons of return loss of whole differential pair, via/solder ball section, and stripline section respectively.

IV. CONCLUSION

This paper has made the efforts on electrical analysis and design of high-speed FC-BGA package with the emphasis on high-speed differential pair. The key factors

in differential pair design that have critical impacts on signal integrity of high-speed package are highlighted and studied. Those include impedance control, and the impact of discontinuities such as via and solder ball. 2D and 3D simulations are carried out to characterize their impacts on the overall packaging performance. Manufacturing tolerance is also considered here. The guidelines extracted in the paper are useful in practical high-speed FC-BGA design.

REFERENCES


